REMARKS

The applicants appreciate the Examiner's thorough examination of the Application and request reexamination and reconsideration of the Application in view of the following remarks.

The Examiner has objected to the drawings because they allegedly should be designated by a legend such as "Prior Art". Applicants herein submit amended Figs. 2 and 2A that each include the designation of the legend "Prior Art". Applicants respectfully request that the Examiner withdraw the objection to Figs. 2 and 2A.

The drawings are also objected to because allegedly they fail to show that one of the output terminals and one of the power supply terminals are connected together and to a single pin as recited in claims 2 and 4. Applicants herein submit an amended Fig. 1 that shows pin 5, which is connected to the V_{ref} output terminal, can also be connected to the V- power supply terminal such that an output terminal and a power supply terminal are connected together and to a single pin, as recited in claims 2 and 4. Support for this amendment can be found in the subject application at page 5, lines 22-23, page 4, lines 15-16, and in claims 2 and 4. Applicants submit that they have addressed the Examiner's objection and respectfully request that the Examiner withdraw this objection to the drawings.

The specification is objected to because allegedly it fails to show the subject matter recited in claims 2 and 4 as described above. Applicants submit that the specification of the subject application at page 5, lines 22-23, and page 4, lines 15-16, provides sufficient support for the features recited in claims 2 and 4. Applicants respectfully request that the Examiner withdraw the objection to the specification.

Claims 1 and 3 stand rejected under 35 USC §103(a) as allegedly being unpatentable over Prior Art Fig. 1 of the subject application in view of U.S. Patent No. 6,445,603 to Abedifard.

The subject invention results from the realization that the underlying problem in degradation of common mode signal rejection with frequency is really due to package capacitance which is the parasitic capacitance developed between a power supply pin and a gain resistor pin and thus the common mode rejection could be dramatically improved by decreasing the effect of the package capacitance which can be done in one or more ways, for example, by spacing each power supply pin an equal distance from a respective one of the gain resistor pins. See the subject application at page 2, line 22 to page 3, line 5.

Fig. 1 of the subject application discloses an integrated circuit chip package 10 that includes pins 1 and 8, labeled RG, which are gain resistor pins to which an external resistance can be connected to set the overall gain of the amplifier. Pins 7 and 4, labeled V+ and V-, are meant to connect to a power supply. See the subject application at page 5, lines 14-19. Because pin 7 is close to pin 8, a parasitic capacitance occurs between these two pins which can decrease the amplifier's common mode rejection ratio at high frequencies. See the subject application at page 7, lines 11-12 and page 6, lines 15-17. Fig. 1 does not disclose or suggest, however, a repatterned integrated circuit chip package including first and second power supply terminals being connected to pins, which are equally spaced from the pins to which first and second gain resistor terminals are connected, as claimed by Applicants.

Abedifard discloses memory chips containing multiple-bank memory devices that

are arranged to be mounted in the memory chips. More specifically, Abedifard is directed to arranging the address and data bond pads in the memory chip to decrease propagation delays. See Abedifard at lines 1-11 of the Abstract; column 3, lines 1-9; and column 7, line 13 - column 8, line 38. Referring to Fig. 3, which the Examiner cites, Vcc and Vss terminals are located on opposite sides of the integrated circuit chip package. The Examiner alleges that it therefore would have been obvious to modify Fig. 1 of the subject invention with the opposing first and second power supply terminals of Abedifard to allegedly provide improvements in die efficiency. However, Abedifard does not disclose or suggest the use of gain resistor pins. Moreover, Abedifard does not disclose or suggest the spacing of Vcc pins and any other pins, much less gain resistor pins, to improve common mode rejection. As noted above, Abedifard is directed towards arranging the bond pads, not the pins of the package.

The combination of Fig. 1 of the subject invention and Abedifard does not result in the subject invention as claimed. Neither reference teaches that the pins to which the first and second power supply terminals are connected are equally spaced from the pins to which the first and second gain resistor terminals are connected, as claimed by Applicants. Fig. 1 of the subject invention clearly does not teach the equal spacing between the power supply pins and the gain resistor pins. Likewise, Abedifard does not teach the equal spacing between the power supply pins and any other pins, and thus does not teach or suggest equal spacing between power supply pins and gain resistor pins. As such, the resulting combination does not provide first and second power supply terminals being connected to pins which are equally spaced from the pins to which said first and second gain resistor terminals are connected, as claimed by Applicants. The resulting

combination of Fig. 1 and Abedifard also would also not produce the benefits of the subject application as claimed, including balancing the effect of package capacitance of a repatterned integrated circuit chip package and reducing the common mode error with frequency.

In contrast to the cited prior art, claim 1 of the subject application recites: "[a] repatterned integrated circuit chip package comprising: first and second power supply terminals; first and second input terminals; first and second output terminals; first and second gain resistor terminals; and a plurality of connection pins on said package for interconnecting with said terminals; said first and second power supply terminals being connected to pins which are equally spaced from the pins to which said first and second gain resistor terminals are connected for balancing the effect of the package capacitance and reducing the common mode error with frequency". Neither Fig. 1 of the subject invention nor Abedifard disclose or suggest first and second power supply terminals being connected to pins which are equally spaced from the pins to which the first and second gain resistor terminals are connected. Claim 3 includes similar features that distinguish over the prior art.

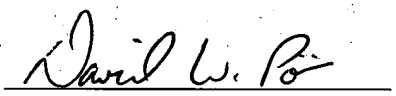
Claims 2 and 4 stand rejected under 35 USC §103(a) as allegedly being unpatentable over Fig. 1 of the subject application in view of Abedifard and further in view of U.S. Patent No. 5,075,633 to Bowers. Bowers shows an instrumentation amplifier. Fig. 2 of Bowers, which the Examiner cites, shows that the V_{ref} and V- terminals may be tied together as indicated by dash line connection 6. Bowers does not disclose or suggest, however, an output terminal and a power supply terminal connected together to a single pin, as recited in claims 2 and 4. Bowers only shows a circuit

diagram and does not show an integrated circuit chip package. Thus, Bowers does not provide the feature recited in claims 2 and 4 of the subject application.

Moreover, since claims 2 and 4 each depend respectively from claims 1 and 3, they are patentable for at least the reasons stated above and are further patentable because they include one or more additional features. Applicants respectfully request that the Examiner withdraw the rejections to claims 2 and 4.

If for any reason this Response is found to be incomplete, or if at any time it appears that a telephone conference with counsel would help advance prosecution, please telephone the undersigned, or his associates, collect in Waltham, Massachusetts, at (781) 890-5678.

Respectfully submitted,



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